Personal System/2
Model 80
Technical Reference

Third Edition (October 1990)

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Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 80 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

- Section 1, "System Overview," describes the system, features and specifications.
- Section 2, "Programmable Option Select," describes registers used for configuration.
- Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

- *IBM Personal System/2 Hardware Interface Technical Reference — Architectures*
- *IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces*
- *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Section 1. System Overview

Notes:

Description

The IBM* Personal System/2* Model 80 is a self-contained, floor-standing computer that features the Micro Channel* architecture. It comes with a keyboard, and can support two internal diskette drives, two internal fixed disk drives, and a tape drive, or CD-ROM.

A system can have either a Type 1, Type 2, or Type 3 system board. The major differences among the three system boards are system clock speed, component layout, and memory. In addition, the Type 3 system board:

- Uses a two-way, set-associative, store-through, 64KB (KB = 1024 bytes) cache for instructions and data
- Has two connectors for system board memory.

Programs identify the type of system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes. The following table shows these bytes, system board types, and system clock speeds.

Model Byte	Submodel Byte	System Board	System Clock
F8	00	Type 1	16 MHz
F8	01	Type 2	20 MHz
F8	80	Type 3	25 MHz

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

System Board Features

The following tables list the system board devices and features. The Hardware Interface Technical Reference manuals describes devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	Type 1 system board, 1 or 2MB (MB = 1,048,576 bytes) Type 2 system board, 2 or 4MB Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	1, 2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode[1] and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Eight channel connectors for Type 3 adapters: - Three 32-bit connectors with a matched-memory extension - Five 16-bit connectors: - One with a video extension - One occupied by the fixed disk drive adapter
Math Coprocessor Socket	---	Supports 80387 math coprocessor Same clock speed as the system microprocessor

[1] The FIFO mode is supported only by the Type 2 serial controller

Figure 1-2. System Board Devices and Features – Type 1 and Type 2

Device	Type	Features
Microprocessor	---	80386 32-bit address and 32-bit data interface
Cache Controller	---	82385 64KB of static-RAM cache
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB
RAM Subsystem	---	4 or 8MB Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 2KB CMOS RAM extension Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output Supports DMA operations
Micro Channel	---	Eight channel connectors for Type 3 adapters: - Four 32-bit connectors with matched-memory extension. - Four 16-bit connectors: - Two with video extension - One occupied by fixed disk adapter.
Math Coprocessor Socket	---	Supports 80387 math coprocessor Same clock speed as the system microprocessor

Figure 1-3. System Board Devices and Features – Type 3

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089 - 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00E0 - 00E2	Memory Encoding Registers
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-4. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock):		
Access to System Board RAM	1	187.5
Access to System Board ROM	1	187.5
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Extended Transfer Cycle	4	375
Refresh Rate (Typically performed every 15.1 μs)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + I/O Access + Memory Access		
Burst Transfers: 375 + (I/O Access + Memory Access)N *		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Extended Transfer Cycle		375
* N is the number of transfers in the burst.		

Figure 1-5. Performance Specifications – Type 1

Device	Number of Waits	Cycle Time (ns)
Microprocessor (20 MHz – 50 ns Clock):		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	100
Memory Read (Page Miss)	2	200
Memory Write (Page Hit)	1	150
Memory Write (Page Miss)	2	200
Access to Channel:		
Default Transfer Cycle	2	200
Synchronous Extended Transfer Cycle	4	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N **		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** N is the number of transfers in the burst.

Figure 1-6. Performance Specifications – Type 2

Device	Number of Waits	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):		
Access to System Board RAM: *		
Memory Read (Cache Hit)	0	80
Memory Write (Cache Hit)	0	80**
Memory Read (Cache Miss, Page Hit)	0 - 2	80 - 160
Memory Write (Cache Miss, Page Hit)	0	80**
Memory Read (Cache Miss, Page Miss)	3 - 5	200 - 280
Memory Write (Cache Miss, Page Miss)	0	80**
Access to Channel:		
Default Transfer Cycle	4	240
Synchronous Extended Transfer Cycle	7	360
Refresh Rate (Typically performed every 15.1 μs)		600 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N ***		
System Board Memory Access		300
Default Transfer Cycle		200
Synchronous Extended Transfer Cycle		300

* Adapters installed in the channel should not rely on monitoring system board memory accesses because channel memory control signals may not be present during these accesses.

** The Write operation is buffered outside the microprocessor. Additional time is required if a Cache Read Miss or another Write operation occurs before the Write operation is completed.

*** N is the number of transfers in the burst.

Figure 1-7. Performance Specifications – Type 3

Size:	
Width	165 mm (6.5 in)
Width (feet extended)	318 mm (12.5 in)
Depth	483 mm (19.0 in)
Height	597 mm (23.5 in)
Weight (with one fixed disk drive)	20.6 kg (45.3 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output:	
225 Watt	350 Watts/hour (1200 BTUs/hour)
242 Watt	375 Watts/hour (1280 BTUs/hour)
250 Watt	390 Watts/hour (1330 BTUs/hour)
Acoustical Readings	(See Figure 1-9 on page 1-11)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.18 kVA
Maximum configuration:	
225 Watt Power Supply	0.58 kVA
242 Watt Power Supply	0.62
250 Watt Power Supply	0.65 kVA
Electromagnetic Compatibility	
FCC Class B	

Figure 1-8. Physical Specifications

Description	L_{WAd} in bels Operation	Idle	L_{pAm} in dB Operation	Idle	$<L_{pA}>_m$ in dB Operation	Idle
Model 80	5.3	5.3	43	43	40	40

Notes

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-9. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drives (per power supply connector)	2.5 A	1.5 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-10. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	16-Bit Connector Maximum Current	32-Bit Connector Maximum Current
+ 5.0 Vdc	1.6 A	2.0 A
+12.0 Vdc	0.175 A	0.175 A
−12.0 Vdc	0.040 A	0.040 A

Figure 1-11. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter

| design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

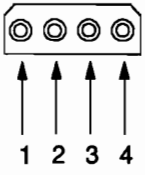
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal fixed disk drives. This connector can be extended to provide power to more than one internal drive as long as the total power does not exceed the connector specifications shown in Figure 1-10 on page 1-12.



Pin	Signal
1	+12 Vdc
2	DC Return
3	DC Return
4	+5 Vdc

Figure 1-12. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 80 system boards.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be set to 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses, hex 0100 through 0107, only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
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0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4 Bit 7 is the channel check active indicator Bit 6 is the channel check status-available indicator
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. POS I/O Address Map

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The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Note: When video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power on. The Type 1 and Type 2 system-boards POST sets it to 1, and the Type 3 system-board POST sets it to 0.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103) – Type 1

This read-only register is accessed while the system board is in the setup mode. It contains information about the presence and type of memory card installed in each system board connector. Connector 1 is closest to the power supply; connector 2 is furthest from the power supply.

Note: The Type 1 system board supports one or two 1MB memory cards.[1]

Bit	Function
7 - 4	Reserved
3	-1MB Memory Card in Connector 2
2	-Memory Card Present in Connector 2
1	-1MB Memory Card in Connector 1
0	-Memory Card Present in Connector 1

Figure 2-6. System Board POS Register 3 (Hex 0103) — Type 1

Bits 7 - 4 Reserved.

Bits 3, 2 These bits indicate if memory is installed in memory connector 2 as shown in the following table.

Bits 3 2	Available RAM
0 0	1MB Memory Card in Connector 2
0 1	Reserved
1 0	Reserved
1 1	No Memory Card in Connector 2

Figure 2-7. POS Register 3 (Bits 3, 2) — Type 1

Bits 1, 0 These bits indicate if memory is installed in memory connector 1 as shown in the following table.

Bits 1 0	Available RAM
0 0	1MB Memory Card in Connector 1
0 1	Reserved
1 0	Reserved
1 1	No Memory Card in Connector 1

Figure 2-8. POS Register 3 (Bits 1, 0) — Type 1

Additional registers at address hex 00E0 and 00E1 are used during setup to define how memory is used. See "Random Access Memory Subsystem" on page 3-12 for more information.

[1] 80386 System Board Memory Expansion Kit.

System Board POS Register 3 (Hex 0103) – Type 2

This read-only register is accessed while the system board is in the setup mode. It contains information about the presence and type of memory card installed in each system board connector. Connector 1 is closest to the power supply; connector 2 is furthest from the power supply.

Note: The Type 2 system board supports one or two 2MB memory cards.[2]

Bit	Function
7 - 4	Reserved
3	2MB Memory Card, Connector 2 (T Signal)
2	-Memory Card Present, Connector 2 (R Signal)
1	2MB Memory Card, Connector 1 (T Signal)
0	-Memory Card Present, Connector 1 (R Signal)

Figure 2-9. POS Register 3 (Hex 0103) – Type 2

Bits 7, 4 These bits are reserved.

Bits 3, 2 These bits indicate if memory is installed in memory connector 2 as shown in the following table.

Bits 3 2	Available RAM
0 0	Reserved
0 1	Reserved
1 0	2MB Memory Card in Connector 2
1 1	No Memory Card in Connector 2

Figure 2-10. POS Register 3 (Bits 3, 2) – Type 2

Bits 1, 0 These bits indicate if memory is installed in memory connector 1 as shown in the following table.

[2] 80386 System Board 2MB Memory Expansion Kit

Bits 1 0	Available RAM
0 0	Reserved
0 1	Reserved
1 0	2MB Memory Card in Connector 1
1 1	Invalid (At Least 1MB Must Be Available in Connector 1)

Figure 2-11. R1 and T1 Bit Values – Type 2

Additional registers at address hex 00E0 and 00E1 are used during setup to define how memory is used. See "Random Access Memory Subsystem" on page 3-12 for more information.

System Board POS Register 3 (Hex 0103) – Type 3

On the Type 3 system board, two read-only registers, POS Register 3 and 4, contain information about the type of memory on the Type 3 system board. The Type 3 system board only supports 80 nanosecond memory cards. The memory connectors are numbered from left to right as viewed from the front of the system. (See Figure 3-34 on page 3-35 for information on the signals.)

Bit	Function
7	Reserved
6	Memory Connector 2 (T2 signal)
5	Memory Connector 1 (T2 signal)
4	Security Override
3	Memory Connector 2 (T1 signal)
2	Memory Card Presence Control (R signal)
1	Memory Connector 1 (T1 signal)
0	Memory Card Presence Control (R signal)

Figure 2-12. System Board POS Register 3 (Hex 0103) – Type 3

Bit 7 This bit is reserved.

Bits 6, 3 These bits indicate the type of memory installed in connector 2 as shown in the following table.

Bits 6 3	Available RAM
0 0	Reserved
0 1	4MB Memory Card in Connector 2
1 0	Reserved
1 1	Reserved

Figure 2-13. POS Register 3 (Bits 6, 3) – Type 3

Bits 5, 1 These bits indicate the type of memory installed in connector 1 as shown in the following table.

Bits 5 1	Available RAM
0 0	Reserved
0 1	4MB Memory Card in Connector 1
1 0	Reserved
1 1	Reserved

Figure 2-14. POS Register 3 (Bits 6, 3) – Type 3

Bit 4, This bit is 0 when the service pin on the speaker/battery connector is connected to ground. This function is used by service and manufacturing personnel.

Bit 2 This is the presence-detect bit for connector 1. This bit is 0 if the proper memory card is installed.

Bit 0 This is the presence-detect bit for connector 2. This bit is 0 if the proper memory card is installed.

System Board POS Register 4 (Hex 0104) – Type 3

On the Type 3 system board, this read-only register and POS Register 3 contain information about the type of memory on the Type 3 system board.

Bit	Function
7	Reserved
6	Reserved
5	- RAM2HS
4	- RAM1HS
3	+ CIDI
2	+ CIDI
1	Reserved
0	+ Disables ROM/RAM 4KB

Figure 2-15. System Board POS Register 4 (Hex 0104) – Type 3

Bits 7, 6, 1 These bits are reserved.

Bit 5 This bit defines the type card installed in connector 2. This bit is 0 if a high-speed (80 nanosecond) memory card is installed.

Bit 4 This bit defines the type card installed in connector 1. This bit is 0 if a high-speed (80 nanosecond) memory card is installed.

Bits 3, 2 These bits are prepared for the memory card of the cache memory controller.

Bit 0 This bit disables the 4KB RAM area starting at E0000 for the display adapter card.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be set up.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-16. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 8 are addressed as 0 through 7, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. The signal, -CD SETUP, goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Section 3. System Board

Description

This section describes the Model 80 implementation of the 80387 Math Coprocessor, Micro Channel architecture, memory subsystem, and miscellaneous system ports. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

80387 Math Coprocessor

The 80387 Math Coprocessors are matched to the speed of the system microprocessor and operate in the synchronous mode. The 16 MHz, 20 MHz, and 25 MHz math coprocessors are not interchangeable; their logical operation is the same.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 80 system boards. Refer to the Micro Channel architecture information in the *Hardware Interface Technical Reference — Architectures* manual for more information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Matched Memory

The 32-bit channel connector with matched-memory extension is a dual 93-pin, 50-mil card-edge design. The matched-memory extension provides three signal lines, two ground lines, and three reserved lines.

Note: Although a memory adapter can respond to -MMC active by driving the '-matched memory cycle request' signal (-MMCR) active, a Type 2 or Type 3 system board ignores -MMCR and performs a default cycle if the 'channel ready' signal (CD CHRDY) is active, or a synchronous-extended cycle if CD CHRDY is inactive. A Type 2 or Type 3 system board will also

drive the '-matched memory cycle command' signal (-MMC CMD) active at the same time as the '-command' signal (-CMD).

Matched-Memory Extension

This extension to the 32-bit Micro Channel connector provides the signals necessary to accommodate matched-memory cycles.

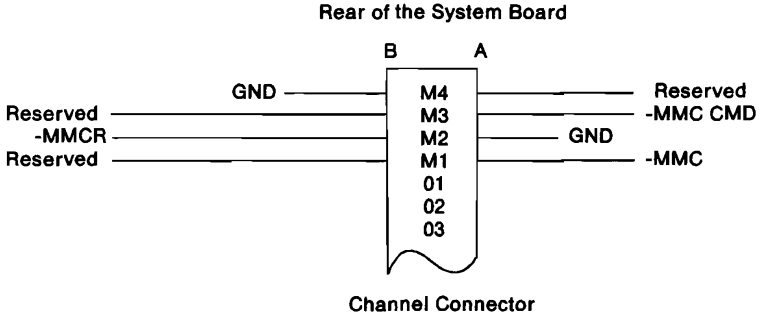


Figure 3-1. Matched-Memory Extension Voltage and Signal Assignments

Signal Descriptions

The following are descriptions of the matched-memory signals.

-MMC: -Matched Memory Cycle: This signal is driven by the system board logic to indicate to the channel slaves that the system microprocessor is the controlling master and is able to run a matched-memory cycle. -MMC is driven by a tri-state driver that can sink 24 milliamps.

-MMCR: -Matched Memory Cycle Request: This is a bus cycle control input signal. A 16- or 32-bit channel slave drives -MMCR to request a matched-memory cycle available on the system bus. This signal is driven active from an address decode and MEMORY/-IO signal.

If -MMCR is driven active by an 8-bit channel slave, or if it is driven active by a 16- or 32-bit channel slave during a cycle other than a microprocessor bus cycle, a default transfer cycle is run and -MMCR is not honored. CD CHRDY is used to extend the matched-memory cycle, as needed. The 'address latch' signal (-ADL) and -CMD remain inactive for the entire matched-memory cycle.

Only the system microprocessor can drive matched-memory cycles. This signal is wired separately to each of the 32-bit channel connectors on the system board and ORed by the system logic. This signal is driven by a totem-pole driver that can sink 6 milliamps.

-MMC CMD: -Matched Memory Cycle Command: This output signal to the bus is generated for system microprocessor bus cycles only. It is used during a matched-memory cycle to define when the data on the bus is valid. The trailing edge of this signal indicates the end of the matched-memory cycle. As with -CMD, this signal indicates the time that the data is valid on the bus, and indicates when to latch the data from the bus or stop driving the data onto the bus. -MMC CMD is driven by a tri-state driver that can sink 24 milliamps.

Matched-Memory Cycle

This section describes the Type 1 matched-memory bus operation supported by the Micro Channel. The Type 1 implementation is such that a channel slave can be either a memory or I/O slave with a data bus width of 16 or 32 bits. No 8-bit devices are allowed to run matched-memory cycles.

In addition to the three basic types of cycles defined by the Micro Channel (default, synchronous extended, and asynchronous extended), the Type 1 system board also supports the matched-memory cycle. The matched-memory cycle is a system-unique function supported by the Micro Channel, and is provided for memory subsystem expansion. This function allows the most efficient data transfer capability between the 16-MHz 80386 system microprocessor and channel memory. The system board ROM and RAM (held on the local bus) and the IBM 80386 Memory Expansion Adapter (held on the channel) adhere to the matched-memory cycle protocol described in this section.

Matched-memory cycles are a minimum of three 16-MHz clocks or a cycle time of 187.5 nanoseconds. (Default transfer cycles are a minimum of four clocks or a cycle time of 250 nanoseconds.) The target channel slave must request the matched-memory cycle on a cycle-by-cycle basis through -MMCR, or it will get the default transfer cycle.

A system microprocessor bus cycle begins by the 'address,' 'byte enables,' and 'bus definition' signals becoming valid in the first clock cycle of the bus cycle. Either of the status bits driven active signals the start of the channel bus cycle. The status state (Ts) is the first clock cycle. After Ts, the command state (Tc) is entered. Channel slaves respond to the bus operation during Tc, either transferring read data to or accepting write data from the system bus. Tc states can be repeated as often as necessary to assure sufficient time for the channel slave to respond. The signal, CD CHRDY, is used to determine whether Tc is repeated. A repeated Tc state is called a 62.5-nanosecond wait state.

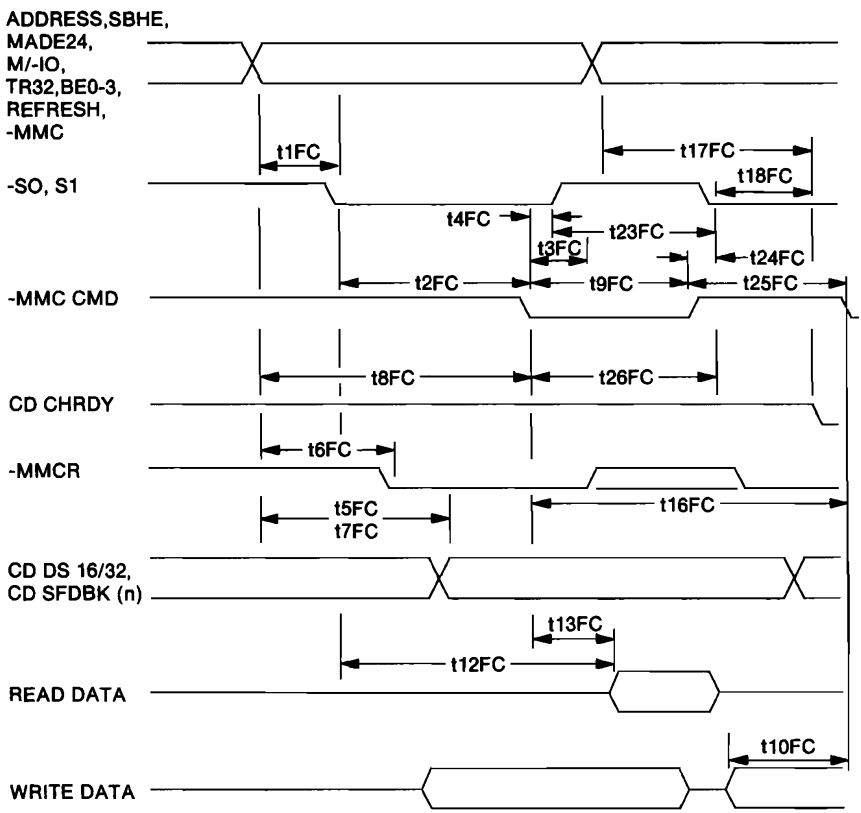
If -MMCR is driven active by the channel slave, then -MMC CMD is driven by the system microprocessor.

If -MMCR is not returned from the channel slave, a default cycle is run. Default transfer and matched-memory bus cycles can be mixed in any manner, because the mechanism is completely dynamic on a

bus cycle basis. Bus cycles can be extended until CD CHRDY is sampled as active.

CD CHRDY is driven inactive by a slave to allow additional time to complete a default or matched-memory cycle when the normal cycle length is not sufficient to service that device. The timings for the matched-memory cycles are shown on the following pages.

Matched-Memory Cycle Timing (No Waits)



Symbol	Description	Min/Max
t3 FC	ADDR hold from -MMC CMD active	20 / - ns
t4 FC	Status hold from -MMC CMD active	25 / - ns
t9 FC	-MMC CMD pulse width	85 / - ns
t9 FCE	-MMC CMD pulse width (Extended Cycle)	145 / - ns
t10 FC	Write data valid to -MMC CMD active	0 / - ns
t11 FC	Write data hold from -MMC CMD inactive	30 / - ns
t13 FC	Read data valid from -MMC CMD active	- / 60 ns
t14 FC	Read data hold from -MMC CMD inactive	0 / - ns
t15 FC	Read data off delay from -MMC CMD inactive	- / 40 ns
t16 FC	-MMC CMD active to next -MMC CMD active	240 / - ns
t17 FC	CD CHRDY valid from ADDR valid	- / 70 ns
t18 FC	CD CHRDY valid from Status active	- / 30 ns
t19 FC	CD CHRDY active from Status inactive	- / 9 ns
t20 FC	Read data valid from -MMC CMD active	- / 125 ns
t21 FC	Read data valid from CD CHRDY active	- / 45 ns
t22 FC	-MMC CMD inactive from CD CHRDY active	65 / - ns
t23 FC	Status inactive pulse width	30 / - ns
t24 FC	Next Status active to -MMC CMD inactive	- / 5 ns
t25 FC	-MMC CMD inactive pulse width	85 / - ns

Figure 3-2. Matched Memory Cycle (No Waits)

Matched-memory cycles are supported for 32-bit and 16-bit channel devices only. Eight-bit channel devices cannot run matched-memory cycles.

Note: Adapters using this protocol can be installed only in the three 32-bit channel connectors and therefore sacrifice some *portability*. These adapters may not fit or operate in some other systems.

When -MMC is active, 32-bit and 16-bit devices should not use -MADE 24, A0, A1, or -SBHE in logic that generates -MMCR, -CD DS 16/32, -CD SFDBK, and CD CHRDY.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following table shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-3. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. To prevent overrun, the diskette drive controller must not be held inactive for more than 12 micro-sections.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and

holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-4. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-5. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit must be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and must be 0.

Bits 3 - 0 These bits are undefined for a write operation and must be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory

The Model 80 systems use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM.

Read-Only Memory Subsystem – Type 1

The ROM subsystem on the Type 1 system board consists of four 32KB by 8-bit modules in a 32KB by 32-bit arrangement (KB equals 1024 bits). ROM is assigned at the top of the first and last 1MB address space (000E0000 and FFFE0000). ROM is not parity-checked. It operates with one 62.5-nanosecond wait state.

Read-Only Memory Subsystem – Type 2 and Type 3

The ROM subsystem on the Type 2 and Type 3 system boards consist of two 64KB by 8-bit modules in a 64KB by 16-bit arrangement. ROM is active at power-on at the top of the first and last 1MB of address space (000E0000 and FFFE0000). After POST ensures the proper operation of system memory, the ROM code is copied to RAM at the same address space, and the ROM is disabled.

Random Access Memory Subsystem

The RAM subsystem on the system board consists of memory modules mounted on a printed-circuit board, which attaches to the system board through a 3- by 32-pin connector. Two connectors are provided on the system board. The Type 1 system board supports the 1MB memory cards; the Type 2 system board supports the 2MB memory cards. Type 2 system board POST routines require a minimum of 1MB of functional memory installed in connector 1. The Type 1 system board requires a minimum of 1MB of functional memory and the Type 3 requires a minimum of 1MB to 4MB; however it can be installed in either connectors 1 or connectors 2. The RAM subsystem is 36 bits wide: 32 data bits and 4 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

Notes:

1. Additional memory can be added in any of the 32-bit Micro Channel connectors. The total amount of memory installed must not exceed the 16MB addressing limit of the DMA controller.
2. For the Type 3 system board, system memory must be 32-bit wide (nonsystem memory can be any width).

System and Nonsystem Memory

Two basic types of memory can be assigned addresses within the memory address space: system memory and nonsystem memory.

System memory is memory that is managed and allocated by the primary operating system. It remains assigned to and fixed in the 4GB (GB = 1,073,741,824 bytes) physical address space, and its contents can be accessed or modified only by an independent master (bus master, system microprocessor, or DMA controller).

Nonsystem memory is memory that is not managed or allocated by the primary operating system. It is made up of memory-mapped I/O devices, memory on an adapter that can be directly modified by the adapter, or memory that can be relocated within the address space, such as bank switched and EMS (expanded memory specifications). Nonsystem memory should not be mapped into microprocessor's cacheable address space.

Memory Caching

The following figure is the memory map for the first 32MB of address space on Type 3 system boards and shows which addresses can be used with the cache. On the Type 3 system board, the address space from 32MB to the end of the second GB (GB = 1,073,741,842 bytes) is not usable. The third and fourth GB are not mapped into the cache, but can be used, especially for nonsystem memory.

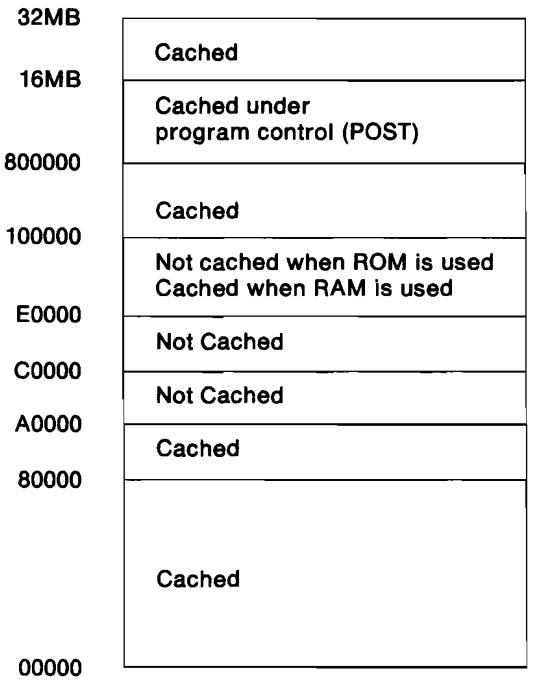


Figure 3-6. Mapping of the First 32MB Segment

Within the first 16MB of address space, all system memory above 1MB must be one contiguous sum starting at the 1MB boundary. If nonsystem memory is present, it should be assigned addresses starting at 16MB and counting down. Do not assign addresses below 8MB to nonsystem memory.

If nonsystem memory exists between 8MB and 16MB, caching for that 8MB block must be disabled even if system memory also is located there. Setup routines must be aware of the existence and location of nonsystem memory so that POST can properly control the caching of the second 8MB.

In the 16MB to 4GB address space, system memory can be contiguously placed from 16MB up to 32MB and can be cached. If nonsystem memory is within the 16MB to 4GB address space, it should be assigned addresses starting at 4GB and counting down, allowing space for system ROM.

Error Recovery

If POST detects a memory error in the first 512KB of memory, the first physical 1MB block of memory is deactivated. The addresses assigned to the deactivated block are reassigned to the second physical block of system board memory, if installed. If an error also is detected in the first 512KB of the second 1MB block of system board memory, the system cannot recover. The first 512KB of memory address space cannot be assigned to reside on an adapter installed in the channel.

POST does not deactivate a memory block if an error is detected in the second 512KB of that block. If an error is detected in that area of memory, the 1MB block containing the error can be deactivated. Have its addresses reassigned by running the memory diagnostics program on the Reference Diskette supplied with the system. Once a block of memory is deactivated, it is ignored by POST.

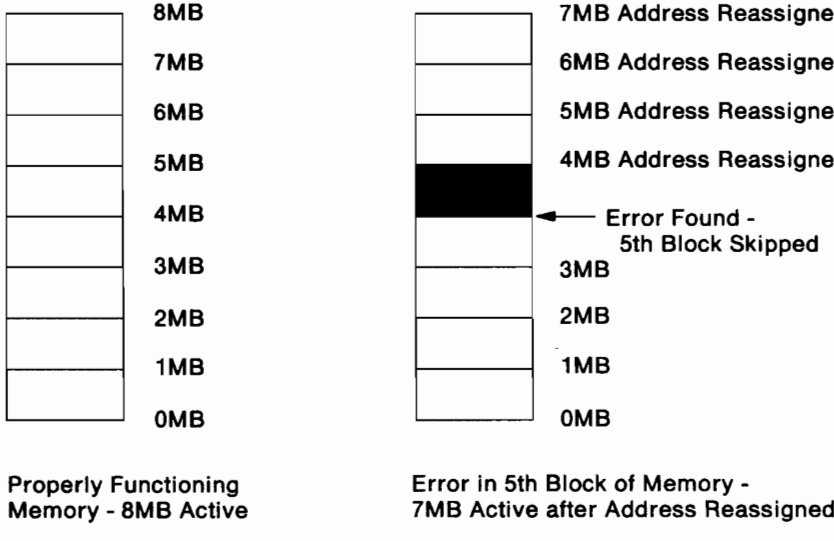


Figure 3-7. Memory Error Address Reassignment

Memory Subsystem Control

The Type 1, Type 2, and Type 3 system boards enable memory in 1MB blocks. Each block must start on a 1MB boundary. Because 128KB of system board ROM, 128KB of I/O ROM, and 128KB of video RAM are mapped within the first 1MB address space, the first physical 1MB of memory cannot be mapped to contiguous addresses and is therefore split at either the 512KB or 640KB boundary. The first 512KB or 640KB is addressed beginning at hex 00000000; the remaining unmapped memory, called the *split-memory block*, can be mapped in several ways:

- Type 1 system board – The entire split-memory block is mapped to the first available address following the last full 1MB block of activated memory. Alternatively, the split-memory block can be handled in either of the following ways:
  - It can be totally disabled.
  - 128KB of the split-memory block can be mapped to the system board ROM address space, replacing the system board ROM. The remainder of the split-memory block is disabled.
- Type 2 system board – In addition to mapping the first 512KB or 640KB of physical RAM, the Type 2 system board automatically maps 128KB of the first 1MB of RAM to the system board ROM address space. The ROM code is then copied into RAM at this location. The remaining unmapped memory, the *split-memory block*, can be either disabled or mapped to the first available address following the last full 1MB block of activated memory .

The size of the split-memory block, memory mapping, and disabling of memory blocks are controlled by registers residing at addresses hex 00E0 and 00E1. The Type 1, Type 2, and Type 3 system boards define these registers differently.

Memory Registers – Type 1

Three registers define how the system board memory is addressed and used:

- Memory Encoding register (hex 00E1)
- Memory Encoding register (hex 00E0)
- Memory Encoding register (hex 00E2).

Memory Encoding Register (Hex 00E1)

This read/write register determines the amount of enabled system board memory and how it is used.

Bit	Function
7	EN4
6	EN3
5	EN2
4	EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-8. Memory Enable Bits (Connector 2)

Bits 7, 6 These bits define the amount of enabled memory in system board memory connector 2.

Bits 7 6	Amount of RAM	Function
0 0	Reserved	
0 1	Reserved	
1 0	1MB	1MB Memory Card enabled in Connector 2
1 1	0MB	Memory Card Disabled or No Memory Card Present in Connector 2

Figure 3-9. Memory Enable Bits (Connector 1)

Bits 5, 4 These bits define the amount of enabled memory in system board memory connector 1.

Bits 5 4	Amount of RAM	Function
0 0	Reserved	
0 1	Reserved	
1 0	1MB	1MB Memory Card enabled in Connector 1
1 1	0MB	Memory Card Disabled or No Memory Card Present in Connector 1

Figure 3-10. Memory Encoding Register (Bits 5 and 4) — Type 1

Bit 3 This bit determines whether the split-memory block is assigned addresses or disabled.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is 384KB or 512KB, depending on the -640 bit, and its address is determined in the Split Address register. When this bit is set to 1, the split-memory block is disabled; however, 128KB of the split-memory block can be used in the ROM address space by setting bit 1 (ROMEN) to 0.

Bit 2 This bit determines where the first active 1MB block of RAM is split.

When this bit is set to 0, 640KB of the first 1MB of memory is mapped into the first 640KB of address space (hex 00000000 to 0009FFFF). When set to 1, 512KB of the first 1MB of memory is mapped into the first 512KB of address space (hex 00000000 to 0007FFFF) and addresses 00080000 through 0009FFFF are unused.

Bit 1 This bit can deactivate the system board ROM and use its address space for system board RAM.

When set to 0, this bit places the ROM address space (hex 000E0000 to 000FFFFF) into RAM. The split-memory block must be disabled. Either 256KB or 384KB of memory is unused (depending on the -640 bit) and the ROM modules are deactivated. When this bit is set to 1, the ROM modules are left active.

The following table shows how bits 3, 2, and 1 are used together to define the various configurations.

Bits 3 2 1	Function
0 0 0	Invalid
0 0 1	ROM Enabled, Split at 640KB, High 384KB at Split Address
0 1 0	Invalid
0 1 1	ROM Enabled, Split at 512KB, High 512KB at Split Address
1 0 0	ROM Disabled, Split at 640KB, 128KB of High 384KB at ROM Address
1 0 1	ROM Enabled, Split at 640KB, High 384KB Not Used
1 1 0	ROM Disabled, Split at 512KB, 128KB of High 512KB at ROM Address
1 1 1	ROM Enabled, Split at 512KB, High 512KB Not Used

Figure 3-11. Memory Encoding – Type 1

Bit 0 When set to 0, this bit enables parity checking of system board memory. To clear a parity error, this bit must be set to 1 and then to 0.

Split Address Register (Hex 00E0) – Type 1

This read/write register defines the starting address of the split-memory block.

Bit	Function
7 - 4	Reserved
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-12. Split Address Register

Bits 7 - 4 These bits are reserved and must be set to 0.

Bits 3 - 0 These bits define the starting address of the split-memory block.

These bits must not be set to a value of 0 unless -ENSPLIT is set to 1. When -ENSPLIT is set to 0, these bits determine the starting address of the split-memory block. The starting address can be at any 1MB boundary from 1MB to 15MB.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Memory Registers – Type 2

Two registers define how the system board memory is addressed and used:

- Memory Encoding Register 1
- Memory Encoding Register 2 (hex 00E0).

Memory Encoding Register 1 (Hex 00E1) – Type 2

This read/write register determines the amount of enabled system board memory in connector 1 and how it is used.

Bit	Function
7, 6	Reserved
5	-Card 1 EN2
4	-Card 1 EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-13. Memory Encoding Register 1 – Type 2

Bits 7, 6 These bits are reserved and must be set to 1.

Bits 5 - 4 These bits define the amount of enabled memory in system board memory connector 1.

Bits 5 4	Amount of RAM	Function
0 0	2MB	2MB Card Enabled in Connector 1
0 1	1MB	First 1MB Disabled on 2MB Card in Connector 1
1 0	1MB	Second 1MB Disabled on 2MB Card in Connector 1
1 1	0MB	Invalid (1MB Minimum Must Be Present)

Figure 3-14. Memory Enable Bits – Type 2

Bit 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space, and the ROM code is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the- 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Bit 2 This bit determines where the first active 1MB of memory is split.

When this bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding register 2.

When this bit is set to 1, the system maps 512KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in Memory Encoding register 2. The addresses, hex 00080000 to 0009FFFF, are unassigned.

Bit 1 This bit determines how addresses, hex 000E0000 to 000FFFFF, are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write addresses are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16-bit accesses to ROM and a longer cycle.

The following figure shows how bits 3, 2, and 1 are used together to define the various configurations.

Bits 3 2 1	Function
0 0 0	ROM Disabled, Split at 640KB, 256KB at Split Address
0 0 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 640KB, 256KB at Split Address
0 1 0	ROM Disabled, Split at 512KB, 384KB at Split Address
0 1 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 512KB, 384KB at Split Address
1 0 0	ROM Disabled, Split at 640KB, 256KB at Split Address Disabled
1 0 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 640KB, 256KB at Split Address Disabled
1 1 0	ROM Disabled, Split at 512KB, 384KB at Split Address Disabled
1 1 1	ROM Enabled (ROM Mapped to RAM Disabled), Split at 512KB, 384KB at Split Address Disabled

Figure 3-15. Memory Encoding Register 1 (Bits 3 and 1)

Bit 0 When set to 0, this bit enables parity checking of system board memory. To clear a parity error, this bit must be set to 1 and then to 0.

Memory Encoding Register 2 (Hex 00E0) – Type 2

This read/write register determines the amount of enabled system board memory in connector 2 and the starting address of the split-memory block.

Bit	Function
7, 6	Reserved
5	-Card 2 EN2
4	-Card 2 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-16. Memory Encoding Register 2 – Type 2

Bits 7, 6 These bits are reserved and must be set to 1.

Bits 5 - 4 These bits define the amount of enabled memory in system board memory connector 2.

Bits 5 4	Amount	Function of RAM
0 0	2MB	2MB Card Enabled in Connector 2
0 1	1MB	First 1MB Disabled on 2MB Card in Connector 2
1 0	1MB	Second 1MB Disabled on 2MB Card in Connector 2
1 1	0MB	All Disabled Or No Card Present.

Figure 3-17. Memory Encoding Register 2 (Bits 5 and 4) – Type 2

Bits 3 - 0 This register defines the starting address of the split-memory block.

These bits must not be set to a value of 0 unless split memory is disabled. When split memory is enabled, these bits determine its starting address. The starting address can be at any 1MB boundary from 1MB to 15MB.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

Memory Registers – Type 3

Memory Encoding registers 1, 2, and 3 define how the system board memory is addressed and used.

Memory Encoding Register 1 (HEX 00E1)

This register determines how the first 1MB of memory is addressed and is used with Memory Encoding Register 2 to determine the amount of system board memory enabled.

Bit	Function
7	-Card 2 EN4
6	-Card EN1
5	-Card EN2
4	-Card EN1
3	-ENSPLIT
2	-640
1	ROMEN
0	-ENPLRPCH

Figure 3-18. Memory Encoding Register 1 (Hex 00E1)

Bits 7, 6 These bits define system board memory in connector 2. When they are set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 Theses bits define system board memory in connector 1. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

BIT 3 This bit determines whether the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the ROM code is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the -640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Note: If the total system memory is equal to or greater than 16MB, the split-memory block cannot be used.

BIT 2 This bit determines where the first active 1MB of memory is split.

When the first bit is set to 0, the system maps 640KB of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 256KB, is mapped to the address specified in Memory Encoding register 2.

When this bit is set to 1, the system maps 512 of the first 1MB to address hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in the Memory Encoding register 2. The address hex 00080000 to 0009FFFF are unassigned.

BIT 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses is assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read addresses are assigned to RAM; the write address are disabled while ROM is disabled.

Note: When this bit is set to 1, system performance will be substantially slower because of 16 bit accesses to ROM and a longer cycle.

BIT 0 When set to 0, this bit enables parity checking of system board memory. For compatibility with other systems, enabling and disabling of parity checking should be done through the System Control Port B at address hex 0061.

Memory Encoding Register 2 (Hex 00E0)

This register is used with Memory Encoding Register 1 to determine the amount of system board memory that is enabled. It also contains the address for the split-memory block.

Bit	Function
7	-Card 4 EN2
6	-Card 4 EN1
5	-Card 4 EN2
4	-Card 3 EN1
3	SPA23
2	SPA22
1	SPA21
0	SPA20

Figure 3-19. Memory Encoding Register 2 (Hex 00E0)

Bits 7, 6 These bits define the system board memory in connector 4. When set to 0, bit 6 enables the first 1MB block and bit 7 enables the second 1MB block.

Bits 5, 4 These bits define the system board memory in connector 3. When they are set to 0, bit 4 enables the first 1MB block and bit 5 enables the second 1MB block.

Bits 3 - 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting address can be at any boundary from 1MB to 15MB.

Memory Encoding Register 3 (Hex 00E2)

This read/write register is used by the Type 3 system board and provides control of the cache memory.

Bit	Function
7	Reserved
6	-Preempt Enable
5	-Cache Flush
4	Lock
3	Reserved
2	-Cache 2nd 8MB
1	Reserved
0	-Enable Cache

Figure 3-20. Memory Encoding Register 3 (Hex 00E2

Bits 7 This bit is reserved.

Bit 6 This bit controls the preempt support for the system microprocessor on the Type 3 system board. When this bit is set to 1, preempt is disabled. When this bit is set to 0, system logic activates the '-preempt' signal when the system microprocessor accesses a memory location not satisfied in the cache (cache miss).

Bit 5 See the description of bit 0.

Bit 4 This bit controls whether locked-access operations from the system microprocessor can or cannot be cache hits. If this bit is set to 0, all locked-access operations are treated as cache misses. If this bit is set to 1, locked access operations can be cache hits.

Bit 3 This bit is reserved.

Bit 2 This bit determines whether the second 8MB of memory is cache are not. When the bit is set to 0, the second 8MB is cache.

Bit 1 This bit is reserved.

Bit 0 This bit and bit 5 work together to control the state of the cache: either disabled and clear, or enabled. These bits must always be opposite polarities, and they must be modified in the same I/O instruction. When bit 5 is set to 0 and bit 0 is set to 1, the cache is disabled and flushed of data; when bit 5 is set to 1 and bit 0 is set to 1, the cache is enabled.

Note: The cache must be disabled and flushed before enabling ROM or disabling the cache of the second 8MB.

System Memory Maps

Memory is mapped by registers at hex 00E0 and 00E1. The mapping results in either 512KB or 640KB of system board RAM starting at address hex 00000000. A 256-byte portion and a 1KB portion of this RAM are reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

In the following tables, the variable *X* represents the number of 1MB blocks of system board memory starting at or above the hex 00100000 boundary. The variable *Y* represents the number of 1MB blocks of memory installed in the channel starting at or above the hex 00100000 boundary (*Y* = 0 to 15).

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 1.

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-21. System Memory Map 1 – Type 1, Type 2, and Type 3

The following table shows the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 1.

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-22. System Memory Map 2 – Type 1, Type 2, and Type 3

The following tables show the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 1
Split address byte = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 512KB - 1)	512KB System Board RAM
(00100000 + *X*MB + *Y*MB + 512KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-23. System Memory Map 3 — Type 1

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB +384KB − 1)	384KB System Board RAM
(00100000 + *X*MB + *Y*MB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-24. System Memory Map 3 — Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 1
Split address byte = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 384KB - 1)	384KB System Board RAM
(00100000 + XMB + YMB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-25. System Memory Map 4 – Type 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to (00100000 + XMB + YMB + 256KB – 1)	256KB System Board RAM
(00100000 + XMB + YMB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM (Same as 000E0000 to 000FFFFF)

Figure 3-26. System Memory Map 4 – Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 1
640 bit = 1
ROM enable bit = 0

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-27. System Memory Map 5 – Type 1

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00008000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-28. System Memory Map 5 – Type 2 and Type 3

The following tables show the memory mapping when:

Enable Split bit = 1
640 bit = 0
ROM enable bit = 0

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-29. System Memory Map 6 – Type 1

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + XMB)	XMB System Board RAM
(00100000 + XMB) to (00100000 + XMB + YMB)	YMB Channel RAM
(00100000 + XMB + YMB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-30. System Memory Map 6 – Type 2 and Type 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 1
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0007FFFF	512KB System Board RAM
00080000 to 0009FFFF	Not Used
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 384KB − 1)	384KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 384KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-31. System Memory Map 7 – Type 2 and Type 3

The following table shows the memory mapping when:

Enable Split bit = 0
640 bit = 0
ROM enable bit = 0
Split address bits = 1 + *X* + *Y* (Total Range = 1 to 15).

Hex Range	Function
00000000 to 0009FFFF	640KB System Board RAM
000A0000 to 000BFFFF	128KB Video RAM
000C0000 to 000DFFFF	Channel ROM
000E0000 to 000FFFFF	128KB System Board ROM mapped to RAM
00100000 to (00100000 + *X*MB)	*X*MB System Board RAM
(00100000 + *X*MB) to (00100000 + *X*MB + *Y*MB)	*Y*MB Channel RAM
(00100000 + *X*MB + *Y*MB) to (00100000 + *X*MB + *Y*MB + 256KB-1)	256KB of First 1MB at Split Address
(00100000 + *X*MB + *Y*MB + 256KB) to FFFDFFFF	Not Used
FFFE0000 to FFFFFFFF	128KB System Board ROM

Figure 3-32. System Memory Map 8 – Type 2 and Type 3

System Board Memory Connectors

The Type 1, 2, and 3 system boards are equipped with two 3- by 32-pin system board memory connectors. A memory card must be installed in connector 1 before additional memory can be used in the channel.

The following figure shows the pin locations of the 3- by 32-pin system board memory connectors. The pin locations are the same for connectors 1 and 2. Connector 1 is closest to the power supply. Pin 32 is closest to the rear of the system board.

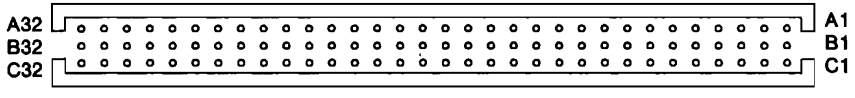


Figure 3-33. System Board Memory Connector Pin Locations

The following is a list of signals used by the system board memory connectors.

-MW -Memory Write

-MA(0 – 8) -Memory Address (0 through 8)

-RAS(0 – 3) -Row Address Strobe (0 through 3)

-CAS(0 – 3) -Column Address Strobe (0 through 3)

-CASP -Column Address Strobe Parity

MDP(0 – 3) Memory Data Parity (0 through 3)

MD(0 – 31) Memory Data (0 through 31)

-BE(0 – 3) -Byte Enable (0 through 3)

R This signal is used by POS Register 3 during system board setup to determine the presence of a memory card in each of the two system board memory connectors.

Note: Type 2 system board POST routines require a minimum of 1MB of functional memory installed in connector 1. The Type 1 system board also requires a minimum of 1MB of functional memory; however, it may be installed in either connector. The Type 3 system board POST routines require 4MB of functional memory installed in connector 1.

-RAMHS This signal is used by POS Register 4 to detect the memory speed.

T1, T2 These signals are used by POS Register 3 during system board setup to determine the type of memory card installed in each of the two Type 3 system board memory connectors. See Section 2, "Programmable Option Select," for additional information.

The following figure shows the pin assignments for the Type 3 system board memory connector. Inputs (I) to and Outputs (O) from the system board also are shown.

Row A			Row B			Row C		
Pin	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**
A1	N/A	Reserved	B1	N/A	Ground	C1	I/O	MD0
A2	O	-MW	B2	O	+5 Vdc	C2	I/O	MD1
A3	O	MA0	B3	N/A	Ground	C3	I/O	MD2
A4	O	MA1	B4	O	+5 Vdc	C4	I/O	MD3
A5	O	MA2	B5	N/A	Ground	C5	I/O	MD4
A6	O	MA3	B6	O	+5 Vdc	C6	I/O	MD5
A7	O	MA4	B7	N/A	Ground	C7	I/O	MD6
A8	O	MA5	B8	O	+5 Vdc	C8	I/O	MD7
A9	O	MA6	B9	N/A	Ground	C9	I/O	MD8
A10	O	MA7	B10	O	+5 Vdc	C10	I/O	MD9
A11	O	MA8	B11	N/A	Ground	C11	I/O	MD10
A12	O	-RAS0	B12	O	+5 Vdc	C12	I/O	MD11
A13	O	-RAS1	B13	N/A	Ground	C13	I/O	MD12
A14	O	-RAS2	B14	O	+5 Vdc	C14	I/O	MD13
A15	O	-RAS3	B15	N/A	Ground	C15	I/O	MD14
A16	I	-RAMHS*	B16	O	+5 Vdc	C16	I/O	MD15
A17	I	-R	B17	N/A	Ground	C17	I/O	MD16
A18	I	T2*	B18	O	+5 Vdc	C18	I/O	MD17
A19	O	-CAS0	B19	N/A	Ground	C19	I/O	MD18
A20	O	-CAS1	B20	O	+5 Vdc	C20	I/O	MD19
A21	O	-CAS2	B21	N/A	Ground	C21	I/O	MD20
A22	O	-CAS3	B22	O	+5 Vdc	C22	I/O	MD21
A23	I/O	MDP0	B23	N/A	Ground	C23	I/O	MD22
A24	I/O	MDP1	B24	O	+5 Vdc	C24	I/O	MD23
A25	I/O	MDP2	B25	N/A	Ground	C25	I/O	MD24
A26	I/O	MDP3	B26	O	+5 Vdc	C26	I/O	MD25
A27	I	-BE0	B27	N/A	Ground	C27	I/O	MD26
A28	I	-BE1	B28	O	+5 Vdc	C28	I/O	MD27
A29	I	-BE2	B29	N/A	Ground	C29	I/O	MD28
A30	I	-BE3	B30	O	+5 Vdc	C30	I/O	MD29
A31	I	-CASP	B31	N/A	Ground	C31	I/O	MD30
A32	I	T1	B32	O	+5 Vdc	C32	I/O	MD31

Note: * Type 3 only

Figure 3-34. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM and 2KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM
000 - 00D	Real-Time Clock
00E	Diagnostic Status
00F	Shutdown Status
010	Diskette Drive Type
011	First Fixed Disk Drive Type
012	Second Fixed Disk Drive Type
013	Reserved
014	Equipment
015 - 016	Low and High Base Memory
017 - 018	Low and High Expansion Memory
019 - 031	Reserved
032 - 033	Configuration CRC
034	Reserved
035 - 036	Low and High Useable Memory
037	Date Century
038 - 03F	Reserved

Figure 3-35. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-36. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-37. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) must be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 must access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS Address register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-38. Real-Time Clock Bytes

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-39. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-40. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read and write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-41. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-42. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

Note: The Setup program initializes status registers A, B, C, and D when the time, and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the registers the same way as the Setup program.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-43. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-44. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-Sided Diskette Drive (48 Tracks Per Inch, 360KB)
0 0 1 1	High-Capacity Diskette Drive (720KB)
0 1 0 0	High-Density Diskette Drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-45. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-Sided Diskette Drive (48 Tracks Per Inch, 360KB)
0 0 1 1	High-Capacity Diskette Drive (720KB)
0 1 0 0	High-Density Diskette Drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-46. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines (for the power-on diagnostic tests) the basic equipment in the system.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-47. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-48. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-49. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-37). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM might occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-50. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-51. System Control Port B (Read)

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer 2 'output' signal.

Bit 4 This bit toggles with each refresh request.

Bit 3 Setting this bit to 0 enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-52. System Control Port A

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT* Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has eight bytes reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can access these bytes only during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from one to seven characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program on the Reference Diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When a power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the "Keyboard and Auxiliary Device Controller" section in the *Hardware Interface Technical Reference*.

Hardware Compatibility

The Model 80 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Model 80 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).

** Intel is a trademark of the Intel Corporation.

- The Intel 8237 DMA controller-address and transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- The Intel 80287 and 8087 math coprocessors.

Error Codes

POST returns a message in the form of a number to indicate the type of test that failed. The following table gives the failure indicated with the associated error code. For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 (this number is for developers who are registered with IBM).

** Motorola is a trademark of Motorola, Incorporated.

Error Number	Error Indication
101	Interrupt failure
102	Timer failure
103	Timer interrupt failure
104	Protected mode failure
105	Keyboard controller command failure
107	Hot MNI test
108	Timer bus test
109	Memory select
110	System board parity
111	I/O parity
112	Watchdog timeout
113	DMA arbitration timeout
114	External ROM checksum
160	System board ID not recognized
161	Bad battery or configuration
162	CMOS checksum or adapter ID mismatch
163	Date and time not set
164	Memory size mismatch
165	Adapter ID mismatch
166	Card busy
167	System clock not updating
201	Memory miscompare or parity
202	Memory address line error (address line 00 - 15)
203	Memory address line error (address line 16 - 31)
211	Memory Base 64K on system board failed
214	Memory Base 64K on daughter/SIP 2 failed
214	Memory Base 64K on daughter/SIP 1 failed
221	ROM to RAM copy
225	Wrong speed memory on system board
301	Keyboard interface
303	Keyboard or system board
304	Keyboard clock failure
305	Keyboard +5V error
601	Diskette Drive or Controller
602	Diskette boot record
1101	Async error
2401	System board video
8601	Mouse timeout
8602	Mouse interface
8603	Mouse interrupt
10480	Drive C seek failure
10481	Drive D seek failure
10482	Drive failed controller test
10483	Driver controller failed to reset
10490	Drive C read failure
10491	Drive D read failure
12901	Failed processor portion of processor board test (Type 3)
12902	Failed cache portion of processor board test (Type 3)

Figure 3-53. Error Codes

Notes:

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